High-speed USB to 4 Serial Port Chip CH9114

Datasheet

Version: V1.1

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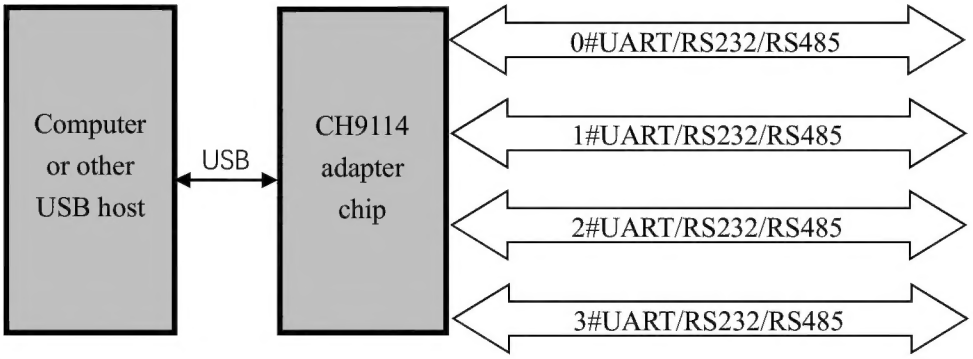
1. Overview

CH9114 is a high-speed USB2.0 bus adapter chip, which realizes high-speed USB to 4 UARTs (UART0/1/2/3) function, and is used to expand UARTs for computers or directly upgrade ordinary serial port devices or MCU to USB bus.

The following figure shows the system block diagram of CH9114.

Figure 1-1 System block diagram

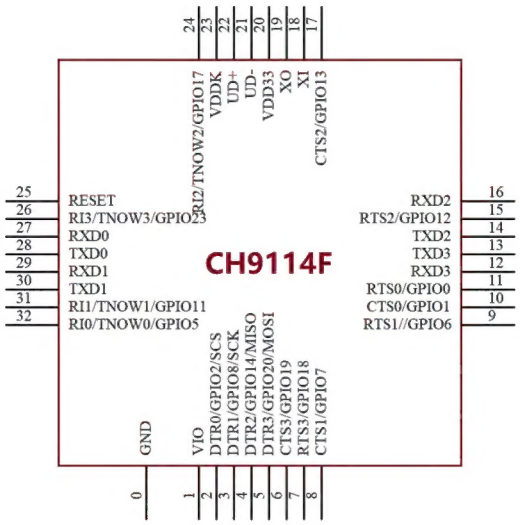


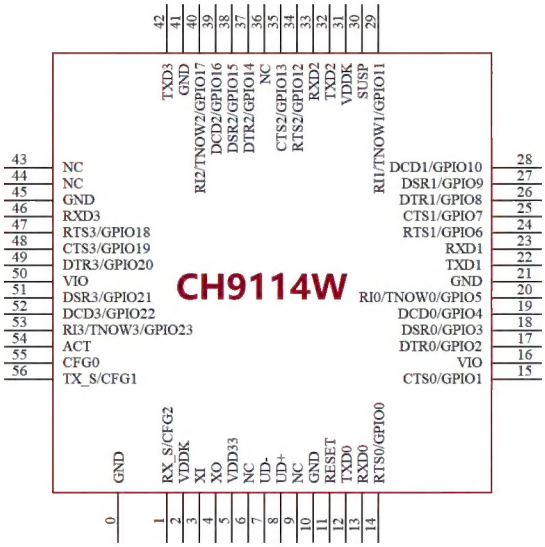
2. Feature

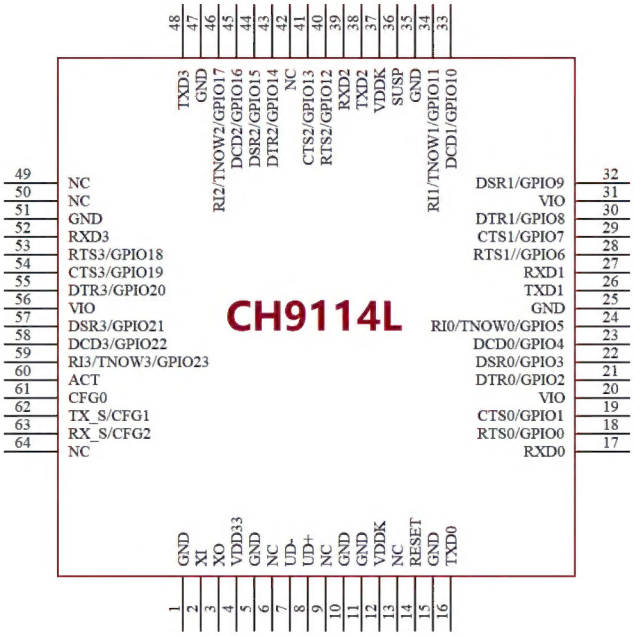
- 480Mbps high-speed USB 2.0 device interface.
- Built-in firmware, simulating standard serial port, used to upgrade the original serial port peripheral equipment, or add additional serial ports through USB.
- The serial port applications under the Windows operating system on the computer side are completely compatible and need not be modified.
- Support installation-free operating system with built-in CDC drivers or multi-functional and high-speed VCP vendor drivers.
- Hardware full-duplex serial port, built-in independent transceiver buffer, supports communication baud rate of 110 bps ~ 15 Mbps.
- The serial port supports 5/6/7/8 data bits, odd parity, even parity, flag bit, blank bit and no parity.
- Each serial port has a built-in receiving FIFO of 8192 bytes and a transmitting FIFO of 4096 bytes.
- Support common MODEM contact signals RTS, DTR, DCD, RI, DSR and CTS.
- Support CTS and RTS hardware automatic flow control.
- Support half-duplex, provide TNOW indicating that serial port is transmitting status, which can be used to control RS485 transceiver switching.
- Support up to 24 GPIO input and output functions.
- By adding level conversion devices, interfaces such as RS232, RS485 and RS422 are supported.
- Built-in EEPROM can configure chip VID, PID, maximum current value, manufacturer and product information string and other parameters.
- Single 3.3V power supply.
- The serial I/O is independently powered and supports 3.3V, 2.5V and 1.8V power supply voltages.

- LQFP64M, QFN56 and QFN32 lead-free packages are available, which are RoHS-compatible.

3. Pinouts







Package Form	Body Size	Pin Pitch		Package Description	Order Model
QFN32	4*4mm	0.4mm	15.7mil	Quad Flat No-Lead Package	CH9114F
QFN56X8	8*8mm	0.5mm	19.7mil	Quad Flat No-Lead Package	CH9114W
LQFP64M	10*10mm	0.5mm	19.7mil	Low-profile Quad Flat Package	CH9114L

Note:

1. The USB transceiver of CH9114 is designed according to USB2.0, and the UD+ and UD- pins cannot be connected in series, otherwise the signal quality will be affected.

2. CH9114F is preferred, which is small in size; CH9114L has many pins, focusing on complete functions.

3. Pin 0# is the EPAD of QFN package and is a necessary connection.

4. Pin Definitions

Pin No. (Pin with the same name can be referenced)			Pin name	Type(1)	Function description
CH9114F	CH9114W	CH9114L			
20	5	4	VDD33	P	3.3V positive power input, external decoupling capacitor is required.
0	0/10/21/41/45	1/5/10/11/15/ 25/35/47/51	GND	P	Common ground terminal, which needs to be connected with the ground wire of USB bus.
23	2/31	12/37	VDDK	P	Core power supply, externally connected with at least 0.1uF decoupling capacitor, 1uF is recommended.
1	16/50	20/31/56	VIO	P	IO pin power input, external supply of 1.8V, 2.5V or 3.3V, external connection of 0.1uF or 1uF capacitor.
25	11	14	RESET	I	External reset input, active low, built-in pull-up resistor
22	8	8	UD+	USB	Directly connected to the D+ data line of USB bus, no additional resistors can be connected in series.
21	7	7	UD-	USB	Directly connected to the D- data line of USB bus, no additional resistors can be connected in series.
18	3	2	XI	I	Crystal oscillation input end
19	4	3	XO	O	Crystal oscillation inverting output terminal
28	12	16	TXD0	O	UART0's serial data output, idle state is high.
27	13	17	RXD0	I	UART0's serial data input, built-in pull-up resistor.
11	14	18	RTS0/ GPIO0	I/0	UART0's MODEM output signal, request to transmit, active low; GPIO0, used for input or output of IO port. If the pin detects an external pull-down resistor during power-on, the configuration parameters in the internal EEPROM are disabled and the default parameters of the chip are enabled.
10	15	19	CTS0/ GPIO1	I/0	UART0's MODEM input signal, clear and transmit, active low; GPIO1, used for input or output of IO port.
2	17	21	DTR0/ GPIO2	I/0	UART0's MODEM output signal, data terminal ready, active low; GPIO2, used for input or output of IO port.
-	18	22	DSR0/	I/0	UART0's MODEM input signal, data device

			GPIO3		ready, active low; GPIO3, used for input or output of IO port.
-	19	23	DCD0/ GPIO4	I/0	UART0's MODEM input signal, carrier detection, active low; GPIO4, used for input or output of IO port.
32	20	24	RI0/ TNOW0/ GPIO5	I/0	UART0's MODEM input signal, ringing indication, active low; UART0's RS485 transmitting and receiving control pins; GPIO5, used for input or output of IO port. During power-on, if it is detected that the pin is externally connected with a pull-down resistor, it is switched to TNOW function, otherwise it is RI function.
30	22	26	TXD1	O	UART1's serial data output, idle state is high.
29	23	27	RXD1	I	UART1's serial data input, built-in pull-up resistor.
9	24	28	RTS1/ GPIO6	I/0	UART1's MODEM output signal, request to transmit, active low; GPIO6, used for input or output of IO port. If it is detected that the pin is externally connected with a pull-down resistor during the power-up of CH9114F chip, all serial ports will automatically enable the hardware flow control function;
8	25	29	CTS1/ GPIO7	I/0	UART1's MODEM input signal, clear and transmit, active low; GPIO7, used for input or output of IO port.
3	26	30	DTR1/ GPIO8	I/0	UART1's MODEM output signal, data terminal ready, active low; GPIO8, used for input or output of IO port.
-	27	32	DSR1/ GPIO9	I/0	UART1's MODEM input signal, data device ready, active low; GPIO9, used for input or output of IO port.
-	28	33	DCD1/ GPIO10	I/0 (FT)	UART1's MODEM input signal, carrier wave detection, active low; GPIO10, used for input or output of IO port.
31	29	34	RI1/ TNOW1/ GPIO11	I/0 (FT)	UART1's MODEM input signal, ringing indication, active low; RS485 transmitting and receiving control pins of UART1; GPIO11, used for input or output of IO port. During power-on, if it is detected that the pin is externally connected with a pull-down

					resistor, it is switched to TNOW function, otherwise it is RI function.
14	32	38	TXD2	0	UART2's serial data output, idle state is high.
16	33	39	RXD2	I (FT)	UART2's serial data input, built-in pull-up resistor.
15	34	40	RTS2/ GPIO12	I/0 (FT)	UART2's MODEM output signal, request to transmit, active low; GPIO12, used for input or output of IO port.
17	35	41	CTS2/ GPIO13	I/0 (FT)	UART2's MODEM input signal, clear and transmit, active low; GPIO13, used for input or output of IO port.
4	37	43	DTR2/ GPIO14	I/0 (FT)	UART2's MODEM output signal, data terminal ready, active low; GPIO14, used for input or output of IO port.
-	38	44	DSR2/ GPIO15	I/0 (FT)	UART2's MODEM input signal, data device ready, active low; GPIO15, used for input or output of IO port.
-	39	45	DCD2/ GPIO16	I/0 (FT)	UART2's MODEM input signal, carrier wave detection, active low; GPIO16, used for input or output of IO port.
24	40	46	RI2/ TNOW2/ GPIO17	I/0 (FT)	UART2's MODEM input signal, ringing indication, active low; RS485 transmitting and receiving control pins of UART2; GPIO17, used for input or output of IO port. During power-on, if it is detected that the pin is externally connected with a pull-down resistor, it is switched to TNOW function, otherwise it is RI function.
13	42	48	TXD3	0	UART3's serial data output, idle state is high.
12	46	52	RXD3	I (FT)	UART3's serial data input, built-in pull-up resistor.
7	47	53	RTS3/ GPIO18	I/0 (FT)	UART3's MODEM output signal, request to transmit, active low; GPIO18, used for input or output of IO port.
6	48	54	CTS3/ GPIO19	I/0 (FT)	UART3's MODEM input signal, clear and transmit, active low; GPIO19, used for input or output of IO port.
5	49	55	DTR3/ GPIO20	I/0 (FT)	UART3's MODEM output signal, data terminal ready, active low; GPIO20, used for input or output of IO port.
-	51	57	DSR3/ GPIO21	I/0 (FT)	UART3's MODEM input signal, data device ready, active low; GPIO21, used for input or output of IO port.

-	52	58	DCD3/ GPIO22	I/0 (FT)	UART3's MODEM input signal, carrier wave detection, active low; GPIO22, used for input or output of IO port.
26	53	59	RI3/ TNOW3/ GPIO23	I/0 (FT)	UART3's MODEM input signal, ringing indication, active low; RS485 transmitting and receiving control pins of UART3; GPIO23, used for input or output of IO port. During power-on, if it is detected that the pin is externally connected with a pull-down resistor, it is switched to TNOW function, otherwise it is RI function.
-	30	36	SUSP	0	USB output in suspend state, active low, output at high level in normal working state, and output at low level after suspend.
-	54	60	ACT	0	USB configuration completion status output, active low.
-	55	61	CFG0	I (FT)	Function configuration pin 0 If it is detected that the pin is externally connected with a pull-down resistor during power-on, all serial ports will automatically enable the hardware flow control function;
-	56	62	TX_S/ CFG1	I/0 (FT)	Serial port data transmission status output Function configuration pin 1 If it is detected that the pin is externally connected with a pull-down resistor during power-on, all RIx/TNOWx pins are configured with TNOW function; otherwise, the RI function and TNOW function are configured by detecting the level of RIx/TNOWx pin during power-on, and the RI function is enabled at high level and TNOW function is enabled at low level.
-	1	63	RX_S/ CFG2	I/0 (FT)	Serial port data receiving status output Function configuration pin 2
-	6/9/36/43/44	6/9/13/42/ 49/50/64	NC	NC	Reserved, suggested suspension

Note 1: Pin type abbreviation explanation:

USB = USB signal pin;

I = Signal input;

O = Signal output;

P = Power or ground;

NC = Reserved;

FT = Tolerant 5V voltage.

5. Function Description

5.1 General Description

CH9114 chip supports 3.3V power supply voltage, and the power supply pins should be respectively connected with power supply decoupling capacitors with a capacity of about 1uF to the ground.
CH9114 chip has a built-in power-on reset circuit. When the chip works normally, it needs to provide a 24MHz clock signal to the XI pin from outside. The clock signal can be generated by the crystal stable frequency oscillation through the inverter built in CH9114. The peripheral circuit needs to connect a 24MHz crystal between the XI and XO pins, and the crystal load capacitance built in the chip is 12pF. If the crystal load capacitance exceeds 20pF, the appropriate load capacitance can be selected according to the crystal requirements.
The external crystal is recommended for CH9114 chip. If the working environment of the chip is relatively ideal and the baud rate error of the serial port can meet the use requirements, the external crystal cannot be soldered. After connecting the XI pin to GND, the chip automatically switches to use the internal clock.
CH9114 chip has built-in all peripheral circuits required by USB bus, including embedded USB controller and USB-PHY, serial matching resistor of USB signal line, 1.5K pull-up resistor required by Device, etc. UD+ and UD- pins can be directly connected to a PC or other USB host. If safety resistors or inductors or ESD protection devices are connected in series for chip safety, the equivalent series resistance of AC and DC should be within 5Ω.

5.2 Serial Description

CH9114 chip provides 4 sets of UARTs (UART0/1/2/3). Each group of serial ports includes TXD, RXD, RI, DSR, DCD, DTR, CTS and RTS, which can realize 3-wire serial port, 5-wire serial port or 9-wire serial port communication.
The pins of CH9114 chip in UART mode include: data transmission pin, MODEM contact signal pin and auxiliary pin.
The data transmission pins include: TXD0, RXD0, TXD1, RXD1, TXD2, RXD2, TXD3 and RXD3. When the serial input is idle, RXDx is high, and when the serial output is idle, TXDx is high.
The MODEM contact signal pin includes: CTS0, RTS0, DTR0, DCD0, RI0, DSR0, CTS1, RTS1, DTR1, DCD1, RI1, DSR1, CTS2, RTS2, DTR2, DCD2, RI2, DSR2, CTS3, RTS3, DTR3, DCD3, RI3, DSR3.
Auxiliary pins include: TNOW0, TNOW1, TNOW2, TNOW3, ACT, SUSP, CFG0, TX_S/CFG1 and RX_S/CFG2, etc. TNOWx is the RS485 sending and receiving control pin corresponding to the serial port. This pin is multiplexed with RIx pin, which is the RIx function by default. During the power-on period, if it is detected that the CFG1 pin is externally connected with a pull-down resistor, all RIx/TNOWx pins are configured with TNOW function, otherwise, the RI function and TNOW function are configured by detecting the level of RIx/TNOWx pins during the power-on period, and the RI function is enabled at high level and TNOW function is enabled at low level. In addition, the RI function and TNOW function can also be selected through EEPROM configuration. ACT is the output pin of USB device configuration completion state, which outputs a high level by default at power-on, and outputs a low level after USB configuration of CH9114 chip by USB host. SUSP pin is output in USB suspended state, which is effective at low level, outputs high level in normal working state, and outputs low level after suspension. CFG0 is the function configuration pin 0. If it is detected that this pin is externally connected with a pull-down resistor during power-on, all serial ports will automatically enable the hardware flow control function. TX_S is the chip serial port to send data status output pin. When any serial port is sending data, the TX_S pin outputs a pulse level with a period of 200 ms. RX_S is the chip serial port receiving data status output pin. When any serial port is receiving data, the RX_S pin outputs a pulse level with a period of 200 ms.

Each serial port of CH9114 chip has built-in independent transceiver buffer, which supports simplex, half-duplex or full-duplex asynchronous serial communication.

The serial data of UART0/1/2/3 includes a low-level start bit, 5/6/7/8 data bits and 1 /2 high-level stop bits, and supports no check/odd check/even check/flag bit/blank bit. Support common communication baud rate: 110, 300, 600, 900, 1200, 2400, 3600, 4800, 9600, 14400, 19200, 28800, 38400, 57600, 76800, 115200, 128000, 153600, 230400, 460800, 921600, 1M, 1.5M, 2M, 2.5M, 3M, 4M, 5M, 6M, 7.5M, 10M, 12M, 15M, etc. When multiple serial ports are used at the same time and the baud rates are different, if the baud rate exceeds 1M, there may be a problem of mutual exclusion, and the baud rate of the serial port opened first is preferred. For example, if UART0 is opened at a baud rate of 5M, other serial ports cannot choose baud rates such as 4M or 6M.

When the baud rate exceeds 1M, the baud rate table that multiple serial ports can be used at the same time is as follows:

Table 5-1 Baud rate for simultaneous use of multiple serial ports

No.	Baud rate at which multiple serial ports can be used simultaneously.
1	1M, 1.5M, 2.5M, 3M, 5M, 7.5M, 15M
2	1M, 1.5M, 2M, 3M, 4M, 6M, 12M
3	1M, 2M, 2.5M, 5M, 10M

The 4 UARTs of CH9114 chip all support CTSx and RTSx hardware automatic flow control, which can be enabled or not enabled at the same time through CFG0 pin configuration (default) or independently configured through VCP vendor drivers. If enabled, the serial port will continue to transmit the next packet of data only when the CTSx pin input is detected to be valid (low level is valid), otherwise the serial port transmission will be suspended; When the receiving buffer is empty, the serial port will automatically activate the RTSx pin (active low), until the data in the receiving buffer is full, the serial port will automatically deactivate the RTSx pin and activate the RTSx pin again when the buffer is empty. Using hardware automatic rate control, you can connect your CTSx pin to the other RTSx pin and send your RTSx pin to the other CTSx pin.

The allowable baud rate error of CH9114 serial port receiving signal is less than 2%, and the baud rate error of serial port transmitting signal is less than 1.5%.

Under the Windows operating system on the computer side, CH9114 supports the CDC class drivers that come with the system, and can also install high-speed VCP vendor drivers, which can simulate the standard serial port, so most serial port applications are completely compatible and usually do not need any modification. In VCP vendor driver mode, it supports up to 24 GPIO input and output control functions.

CH9114 can be used to upgrade the original serial peripheral equipment, or to add additional serial ports to the computer through USB bus. By adding level shifting devices, interfaces such as RS232, RS485 and RS422 can be further provided.

5.3 Chip Parameter Configuration

The manufacturer identification code VID, product identification code PID and product information of CH9114 can be customized when it is used in a large lot.

In a few applications, the built-in EEPROM can be used for parameter configuration. After installing the VCP manufacturer driver, the user can flexibly configure the parameters of the chip such as the manufacturer identification code VID, product identification code PID, maximum current value, BCD version number, manufacturer information and product information string descriptor through the configuration software CH34xSerCfg.exe provided by the chip manufacturer.

6. Parameters

6.1 Absolute Maximum Value (Critical or exceeding the absolute maximum value will probably cause the chip to work improperly or even be damaged)

Name	Parameter Description	Min.	Max.	Unit
T_A	Ambient temperature during operation	-40	85	℃
T_S	Ambient temperature during storage	-40	105	℃
V_{DD33}-GND	Power supply voltage (V_{DD33})	-0.4	4.0	V
V_{IO}-GND	I/O supply voltage (V_{IO})	-0.4	4.0	V
V_{USB}	Voltage on USB signal pin	-0.4	V_{DD33}+0.4	V
V_{IO5V}	Voltage on the I/O pin of tolerant 5V	-0.4	5.5	V
V_{UART}	Voltage on serial port and other pins	-0.4	V_{IO}+0.4	V

6.2 Electrical Parameters (Test conditions: T_A=25℃, V_{DD33}=3.3V, VIO = 3.3V, no USB pin)

Name	Parameter Description	Min.	Typ.	Max.	Unit
V_{DD33}	Power supply voltage (V_{DD33} pin supplies power, GND pin is grounded)	3.0	3.3	3.6	V
V_{IO}	I/O pin supply voltage	1.7	3.3	3.6	V
I_{CC}	Power supply current when the chip works normally	20	30	40	mA
I_{SLP}	Power supply current when USB is suspended	200	300	450	uA
V_{IL}	Low level input voltage	0		0.7	V
V_{IH}	High level input voltage	2.0		V_{IO}	V
V_{IH5}	High-level input voltage of tolerant 5V pin.	2.0		V_{IO}	V
V_{OL}	Output low voltage, and input 5mA current in a single pin.		0.4	0.6	V
V_{OH}	Output high level, and outputs 5mA current in a single pin.	V_{IO}-0.6	V_{IO}-0.4		V
R_{PU}	Equivalent resistance of built-in pull-up	30	40	55	KΩ
V_{POR}/V_{PDR}	Threshold voltage of V_{DD33} power-on/power-off reset	2.55	2.7	2.85	V
V_{ESD}	ESD electrostatic tolerant voltage (HBM, non-contact)		6		KV

6.3 Timing Parameters (Test conditions: T_A = 25℃, V_{DD33} = 3.3V)

Name	Parameter Description		Min.	Typ.	Max.	Unit
FD	Internal clock error (year-on-year effect on baud rate)	T_A = 0℃~70℃	-1.2		1.7	%
		T_A = -40℃~85℃	-2.2		2.2	%
T_{RSTD}	Reset delay after power-on or external reset input.		15	30	45	mS
T_{SUSP}	Detecting USB automatic suspension time		3	5	9	mS

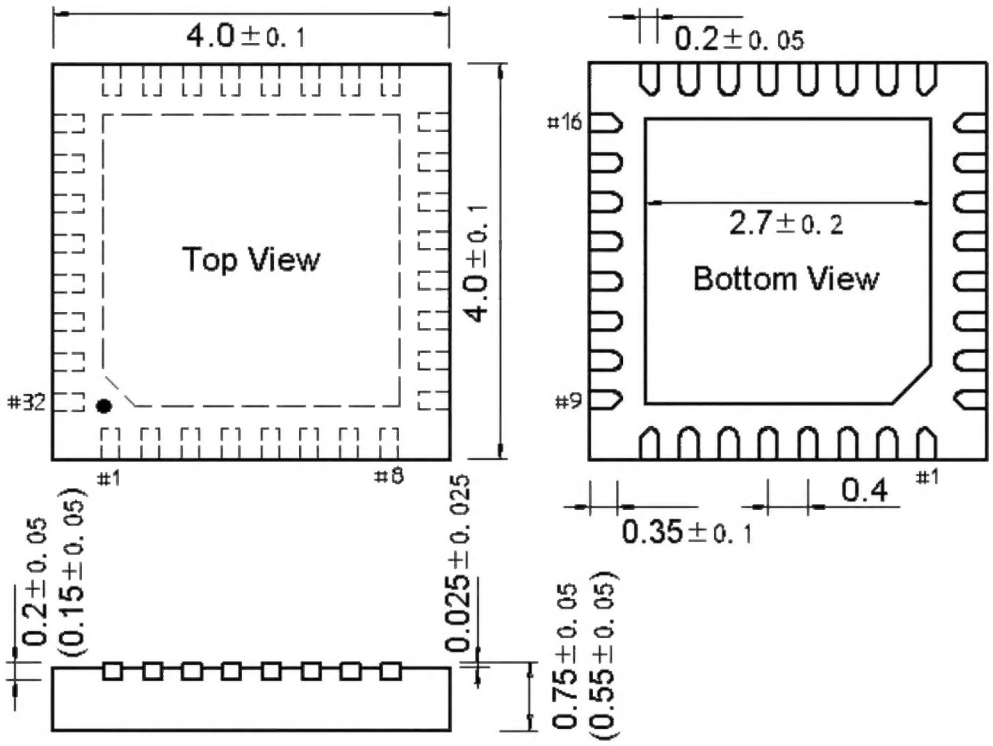
T_{WAKE}	Wake-up completion time after chip sleep	0.3	0.5	4	mS

7. Package Information

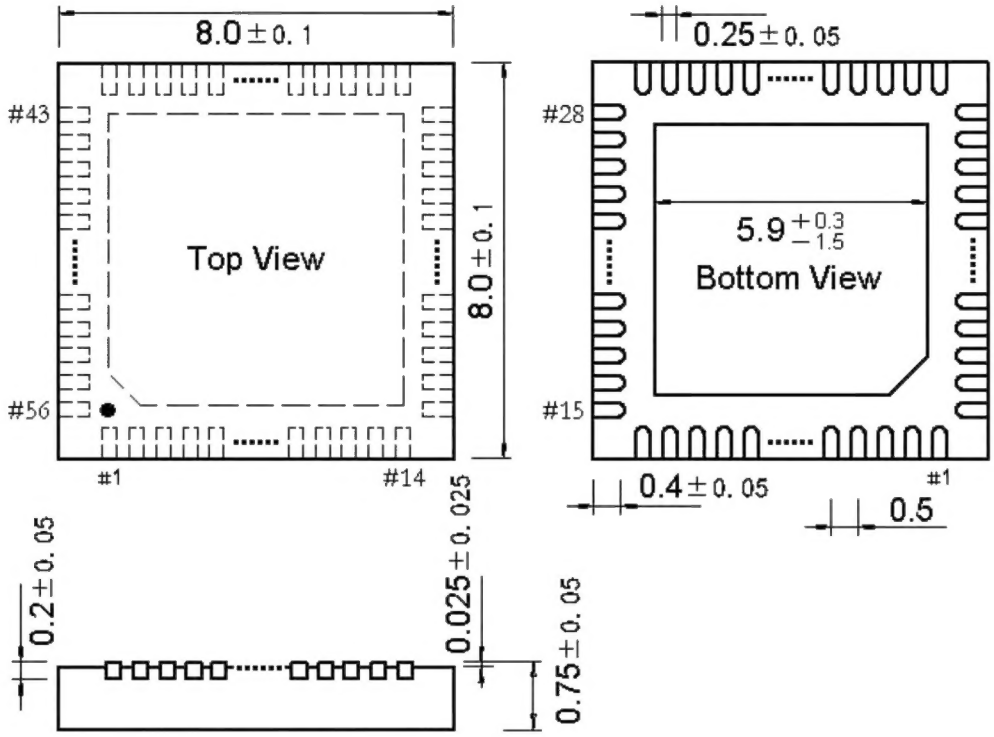
Note: All dimensions are in millimeters.

The pin center spacing values are nominal, without error. And the error of dimensions other than the pin center spacing values is not more than ±0.2mm.

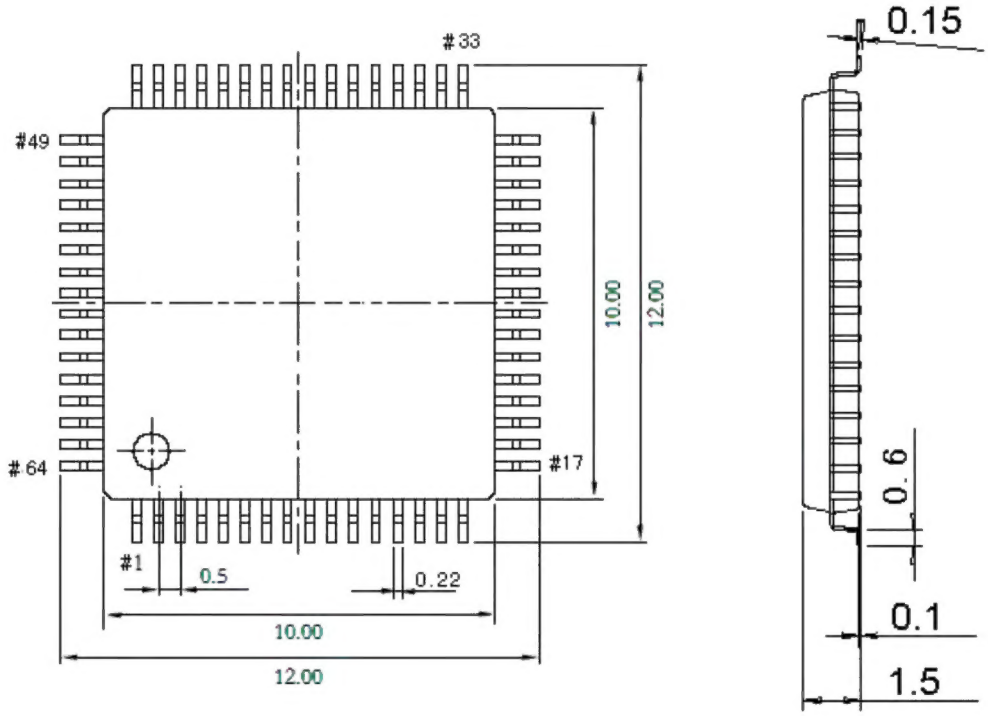
7.1 QFN32 Package



7.2 QFN56X8 Package



7.3 LQFP64M Package



8. Applications

8.1 USB to 4-channel TTL Serial Port

Figure 8-1 below is the reference circuit diagram of high-speed USB to four-way TTL serial port realized by CH9114 chip. The signal lines in the figure can only be connected to RXDx, TXDx and common ground, and other signal lines CTSx, RTSx, DTRx, DSRx, RIx/TNOWx and DCDx can be selected as needed, and they can all be suspended when not needed.

P1 is a USB port, and the USB bus includes a pair of 5V power lines and a pair of data signal lines. Usually, the +5V power line is red, the grounding line is black, the D+ signal line is green, and the D- signal line is white. The power supply current provided by USB bus can reach 500mA.

P2, P3, P4 and P5 are TTL connection pins of each serial port, including VIO, GND, RXDx, TXDx, RTSx, CTSx, DTRx, DSRx, RIx/TNOWx and DCDx. A level shifter can be added to realize the signal conversion from TTL to RS232, RS485 and RS422.

CH9114 chip supports 3.3V power supply voltage, and each power supply pin should be externally connected with a power supply decoupling capacitor, as shown in the figure, C7, C8, C9, C10, C11 and C12 are the power supply decoupling capacitors.

It is suggested to add ESD protection devices for USB signal lines. The parasitic capacitance of ESD chip should be less than 2pF, such as CH412K, and its VDD33 should be connected to 3.3V.

It is suggested that the serial peripheral and VIO of CH9114 chip use the same power supply.

When designing a printed circuit board PCB, it should be noted that decoupling capacitors C7, C8, C9, C10, C11 and C12 should be as close as possible to the power supply pin connected to CH9114; The D+ and D- signal lines of USB port are wired in parallel according to the high-speed USB specification, so as to ensure the characteristic impedance, and try to provide ground wires or copper-clad on both sides to reduce the signal interference from the outside.

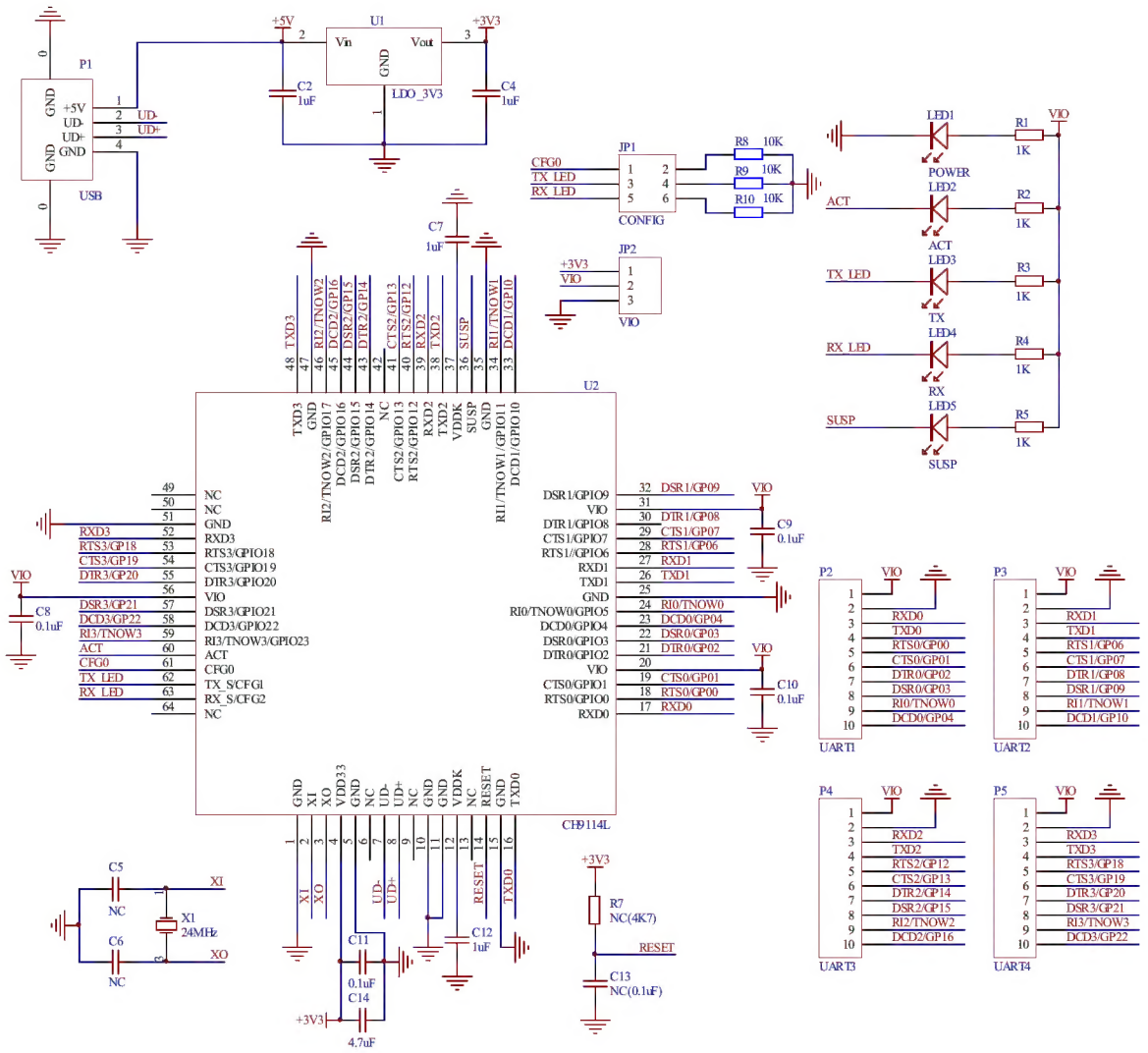



Figure 8-1 Reference circuit diagram of high-speed USB to 4-channel TTL serial port